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Quantum-Dot Cellular Automata bases 4-Bit Binary Adder Design

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Abstract: : The main goal of this work is to develop and implement a 4-bit binary adder based on Quantum-Dot Cellular Automata (QCA). An integral part of digital computer systems, the adder is necessary to execute arithmetic operations on binary values. In this project, several adder circuit components—such as inverters, half adders, full adders, and a 4-bit binary adder made up of several full adders—are created utilising QCA technology. Several methods, including cascading several adder modules and using logic gates and transmission gates, are used in the implementation. The significance of this study is in designing high-performance and compact adder circuits by utilising the special qualities of QCA, such as ultra-fast computation, energy efficiency, and scalability. The goal of the research is to show the benefits and viability of using QCA-based computing for arithmetic operations, clearing the path for the creation of strong and effective computer systems. Key findings from earlier studies in QCA-based computing are compiled through an extensive literature review, offering a strong basis for the endeavour. The literature review includes contemporary developments in adder design and optimisation utilising QCA in addition to classic publications on QCA technology. The project involves using QCA-based simulation tools to create and simulate several adder components. Through simulation tests, the adder circuits' functionality and performance are assessed, offering important insights into how well they work. Additionally, a thorough examination of the suggested adder designs is provided, emphasising their benefits and their uses in digital computing systems.

Keywords: QCA, Full adder, 4 bit binary adder, half adder.

1. Introduction

Effective arithmetic operations comprise the cornerstone for various digital computing applications, from basic calculators to intricate computational jobs. The adder, which adds two binary numbers and any carry created during the process, is one of the essential parts that makes these operations possible. Complementary metal-oxide-semiconductor (CMOS) technology is widely utilised to create traditional adders; however, new paradigms such as Quantum-Dot Cellular Automata (QCA) present intriguing substitutes with distinct benefits.QCA is a nanotechnology-based computing paradigm that leverages the quantum properties of electron charge and tunneling phenomena to perform logic operations. Compared to CMOS Technology, Ultra-fast operation, low power consumption, and intrinsic nanoscale scalability are just a few advantages of QCA technology. Because of these features, QCA is especially well suited to the implementation of high-performance arithmetic circuits, like adders.

The main goal of this project is to leverage The main goal of this project is to leverage QCA technology to develop and build a 4 – bit binary adder. The 4- bit adder is selected because it is an essential component for executing moderately precise arithmetic operations on binary integers. We can show arithmetic operations by building a 4- bit adder, which paves the way for more sophisticated computational systems. This project's introduction aims to give a general overview of the project's purpose. Its goals , and the organization of the research, such as the design, simulation, and analysis of the QCA-based 4-bit binary adder, and it shows the importance of QCA technology in the context of digital computing. In addition, the introduction provides a quick overview of the major adder design elements such as inverters, half adders, and full adders setting the stage for the in-depth analysis that takes place in the ensuring parts.

The introduction basically acts as a primer, introducing the reader to the project's goals and scope and setting the stage for the discussions that follow on QCA technology, adder design concepts, implementation techniques, and

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performance evaluation. We hope that this initiative will further the development of QCA-based computing and open the door for its eventual incorporation into digital systems in the future.

This paper is structured as follows. Shown in Section 2 (Literature Survey), provided in Section 4 (Proposed Method), and covered in Section 3 (QCA Fundamentals). Simulation Results were examined in Section 5 and again in Section 6 (Conclusion).

2. Literature Survey

Cellular Automata (QCA) are covered in the literature survey that is supplied. These studies are especially relevant when developing adders and delving into the basic ideas of QCA technology. Below is a detailed examination of every paper that incited: The foundation for later studies in the field of Quantum Cellular Automata (QCA)" is laid by this groundbreaking article. It goes over the fundamentals of QCA and looks into possible uses in computers and nanotechnology.[1]

This book offers a thorough introduction to nanotechnology, covering both its foundational science and its newest applications. Although not specifically related to QCA, it probably provides insightful background knowledge on nanoscale phenomena and tools that are important to QCA study.[2]

The quasiadiabatic switching mechanism for metal-island quantum-dot cellular automata is studied in this study. It examines methods for obtaining dependable and effective switching operations in circuits based on QCAs, which is necessary for real-world application.[3]

This paper reports on a study on Quantum-Dot Cellular Automata implementations of adder circuits. It probably covers design processes, performance assessment, and possible uses for QCA-based adders.[4]

The principles and possible uses of Quantum Cellular Automata are explored in this work as it explores the physics of computing with arrays of quantum dot molecules. It probably sheds light on the fundamental physics guiding QCA operation..[5]

This work investigates new complete adder designs made especially for Quantum-Dot Cellular Automata technology. It probably offers performance assessments, novel circuit designs, and optimization methods for QCA-based full adders.[6] This work suggests a novel QCA-based architecture for fault-tolerant full adders. It probably looks into ways to improve the fault tolerance and dependability of QCA-based adder circuits, which are essential for real-world applications.[7]

An optimized complete adder design based on Nanoscale Quantum-Dot Cellular Automata is presented in this work. It probably covers methods for enhancing QCA-based full adders' functionality, power economy, and space usage.[8]

In this paper, a high-performance architecture for Quantum-Dot Cellular Automata complete adders is proposed. Most likely, it concentrates on improving signal routing, layout design, and circuit parameters in QCA-based adder circuits to get better performance.[9]

This paper examines the energy dissipation properties of a complete adder structure in Quantum-Dot Cellular Automata without cross-wiring.

It most likely looks on cutting-edge design strategies for QCA-based adder circuits to lower energy consumption and boost efficiency.[10]

By providing insights into circuit design, optimization strategies, fault tolerance mechanisms, and future applications in computers and nanotechnology, these research jointly enhance the field of Quantum-Dot Cellular Automata technology.

3. Introduction

Another perspective on nanotechnology is Quantum-Dot Cellular Automata (QCA), which encodes double data by charging a phone instead of using conventional current switches.

Since the columbic cooperation between the electrons is sufficient for calculation, there is no stream inside the cells. This perspective provides one of several possible solutions for nanoscale transistor-less computation.

Two electrons and four quantum dots make up a conventional QCA cell [16]. A six-dot and an eight-dot QCA cell are two of the several dots of QCA cells that have been proposed. Due to a shared shock of like charges, two electrons in a QCA cell have askew inverted regions in the cell.

Figure illustrates an example of a simple unpolarized QCA cell made up of four quantum dots arranged in a square. In essence, 1 dots are locations where a charge can be restricted. Two extra electrons are present in the cell and are free to go between the four spots.

Suffocating burrowing into or out of a cell. The dot on the upper right corner of the cell is the starting point for the clockwise numbering of the dots. This technology provides non-destructive, real-time, and affordable detection with the potential for enhance food safety and standards.

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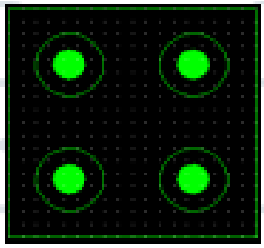

Fig.1 Simple 4-dot Unpolarized QCA cell

Therefore, the definition of a polarisation P in a cell, which quantifies how evenly the electronic charge is spread across the four dots, is as follows:

Where pi is the e- charge in each dot of a 4dot

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

QCA division. Depending on the polarization of the charges within the cell, a QCA cell can exist in either of the two states once it has polarized. As illustrated in Fig. 2, the two most likely polarization states of QCA can be designated as P = +1 and P = -1 due to columbic repulsion. Because of the very slim (almost nonexistent) chance that an incorrect state could exist, the two polarization states shown above are referred to as the most likely rather than the only two.

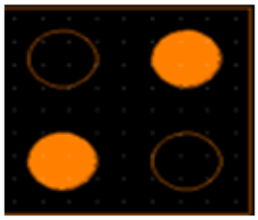

Figure.2 P = +1 Binary Logic1 P = - 1 Binary Logic 0

3.1. Basic Logical devices in qca

As was discovered in earlier sections, columbic cooperation between nearby QCA cells allows data in those cells to be shared; the state of one cell affects the state of the other. The key justification devices in QCA are:

3.1.1. Logical Devices in QCA

As was discovered in earlier sections, columbic cooperation between nearby QCA cells allows data in those cells to be shared; the state of one cell affects the state of the other. The key justification devices in QCA are: Binary Wires, Inverter, Majority Gate Vote

3.1.2. Binary Wire

To transfer data, a paired wire is an even arrangement of cells that starts with one and moves on to the next. A QCA wire example can be found in Figure 3. To ensure that the flag doesn't break apart, a parallel wire is routinely divided into several clock zones. This is because signs typically deteriorate with a lengthy chain of cells in a similar timing zone.

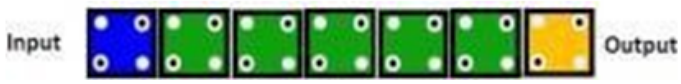

Figure.3 A QCA binary wire Realization

3.1.3. Inverter

The polarisation of two cells positioned diagonally will be opposite. It is now possible to create inverters using lines of cells that are aligned diagonally. Figure illustrates a QCA inverter in action.

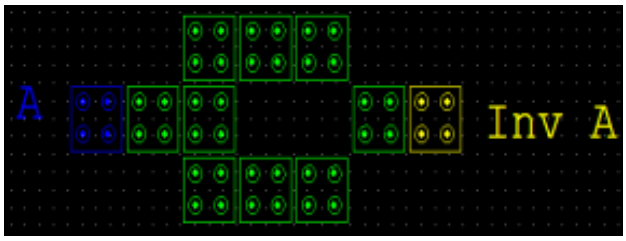

Figure.4 QCA designed inverter circuits

3.1.4. Majority Gate

In a QCA design, the Majority Gate (MV) is the basic logic block. Five cells can be used to create a majority gate. The input cells are the top, left, and bottom ones. The cell on the right will get the majority of the input bits from the device cell. Figure 5 provides an example of an MV representation in QCA.

Figure.5 A three input majority Gate

3.2. QCA Clock

This section will explain and discuss the operation of the QCA clock. The QCA clock contains more stages than just a high and a low, in complete contrast to the conventional CMOS clock. The QCA clock's eras and its pictures are discussed below. There are several steps in the QCA check. It is not possible to plan individual QCA cells separately. The disentanglement gained by the QCA design's inherent neighbourhood connectedness might easily be overwhelmed by the wiring needed to clock each phone separately [8]. For distinct clock zones, four phase switching is implemented in every clocking phase. Throughout the four clock zones, information is piped

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from inputs to outputs.

3.3. Crossing

For improved stability in QCA structures, the fabrication of component interconnections must be managed well. There are now two distinct crossover types available. They are layered and coplanar. Similar to CMOS circuit design, multilayer crossover uses numerous layers to connect its component parts. Two distinct cells cross the wire in a coplanar crossover technique. Because these cells are orthogonal to one another, their actions have no effect on nearby cells. As seen in Figure 8, the first wire has cells with 900 orientations, while the second wire only has 450 orientations. This scheme's primary disadvantage is that any fabrication-related misalignment of the cells could result in a cross-coupling between the two wires. Although efforts have been made to lessen these impacts and strengthen the circuits' resilience, all of these have resulted in significant overhead [14, 19].

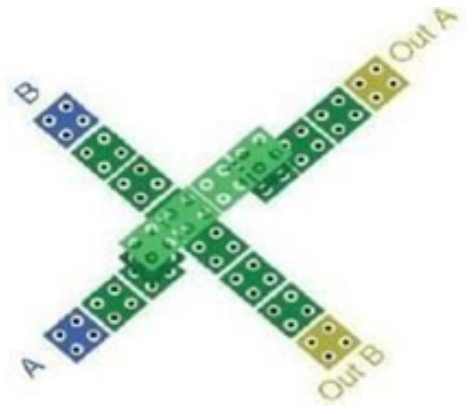

Figure.8 Crossover diagram different orientation

S. H. Shin [21] discusses another kind of coplanar wire crossing in detail. As seen in Figure 8, the first wire has cells with 900 orientations, while the second wire only has 450 orientations. This scheme's primary disadvantage is that any fabrication-related misalignment of the cells could result in a cross-coupling between the two wires.

There are two varieties of crossovers in existence. They are layered and coplanar. Wire crossing is based on interference of clocking phases as depicted in Figure

4. Process and Method

4.1. Inverter Using Transmission Gate

Ensures low power consumption and fast switching speeds, essential for QCA-based circuits.

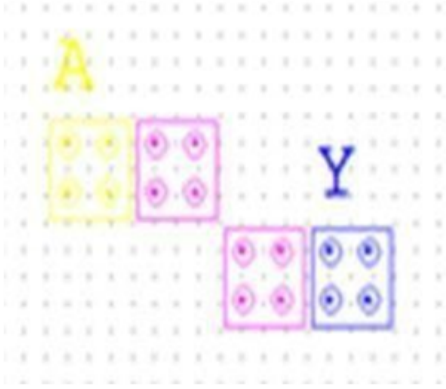

Figure.9 Inverter using transmission gate

Table.1 Inverter Truth table

Input A	Output X
0	1
1	0

Figure 9 probably shows the circuit layout or schematic design of an inverter in the context of Quantum-Dot Cellular Automata (QCA) technology that uses a transmission gate. An inverter is a basic logic gate in QCA that produces its complement as the output by reversing the polarity of the input signal. transmission with the least amount of energy loss.

A pass transistor and a control gate are the two primary parts of an inverter that uses a transmission gate. When the control gate is active, the pass transistor permits the input signal to flow through, but when it is not, it blocks it. The polarity of the input signal can be reversed to create the complement of the input signal by adjusting the state of the control gate. As a result, the inverter's truth table would indicate that an input signal of 0 corresponds to an output signal of 1, and vice versa. This truth table offers a concise illustration of the inverter circuit's functionality and acts as a guide for confirming its performance under various conditions.

4.2. Inverter Using Gates

An inverter that makes use of logic gates is a fundamental component in digital circuit design, particularly Quantum-Dot Cellular Automata (QCA). Here's how to make an inverter and describe how it operates using logic gates: In a traditional logic gate-based inverter, the NAND or NOR gates are the most often used gates. Both gates can be configured to function as inverters by properly connecting their inputs and outputs.

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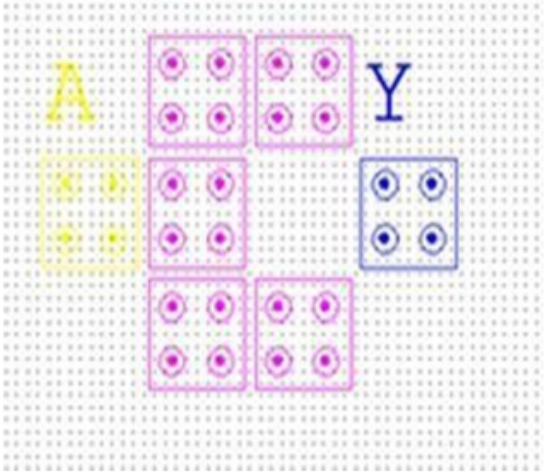

Figure.10 Inverter using logic gates

This other method uses ordinary logic gates, such as NAND or NOR gates, to create inverters. To obtain the desired signal inversion functionality, the gates may need to be configured as part of the design. Compared to transmission gate-based inverters, this method may result in somewhat higher power consumption, even if it may offer more circuit design freedom.

4.3. HALF ADDER

The schematic diagram or circuit layout of a half adder used in Quantum-Dot Cellular Automata (QCA) technology is most likely shown in Figure 11. A half adder is a simple digital circuit that generates the total and carry-out outputs by adding two single-bit binary values. Using QCA cells that are set up to carry out the necessary logic operations, the half adder is realised in QCA. The circuit architecture presented in Figure 11 most likely consists of QCA cells, which stand for AND XOR gates, the two basic components of a half adder. Based on the input binary integers, these cells collaborate to calculate the sum and perform outputs.

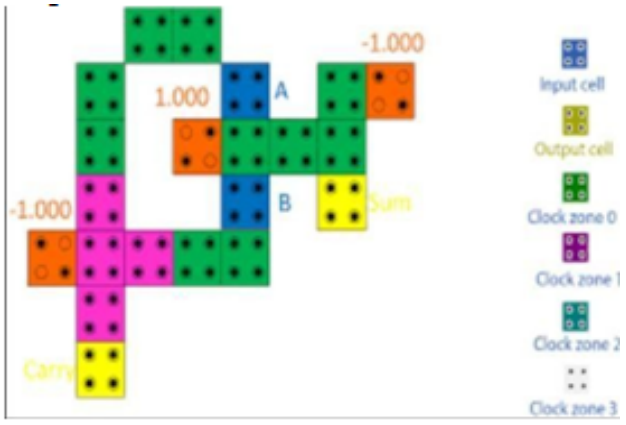

Figure.11 Half adder

The truth table for the half adder circuit shown in Figure 11 is most likely presented in Table II. The relationship between the binary integers (A and B) that are input and the final sum (S) and carry-out (C_out) outputs is specified in the truth table. A distinct input combination is represented by each row in the truth table, and the associated outputs are stated. Based on the input binary integers, these cells collaborate to calculate the sum and perform outputs. To add two single-bit binary values, the half adder is implemented using QCA cells.

Table.2 Half Adder Truth Table

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

QCA cells are used in the implementation of the half adder to add two single-bit binary values. The half adder function is realised by the design and integration of QCA-based XOR and gates. This part comprises the basis of the 4-bit binary adder architecture and is the fundamental building block for developing higher-level adders.

4.4. Full Adder

A schematic or layout of a full adder circuit based on Quantum-Dot Cellular Automata (QCA) is most likely shown in Figure 12's full adder design. The sum (S) and the carry-out (C_out) are the two outputs of a complete adder, which is a digital circuit that adds three input bits (A, B, and a carry-in, or C_in). The way the QCA cells are set up allows them to carry out the logical operations required to calculate the sum and carry out bits.

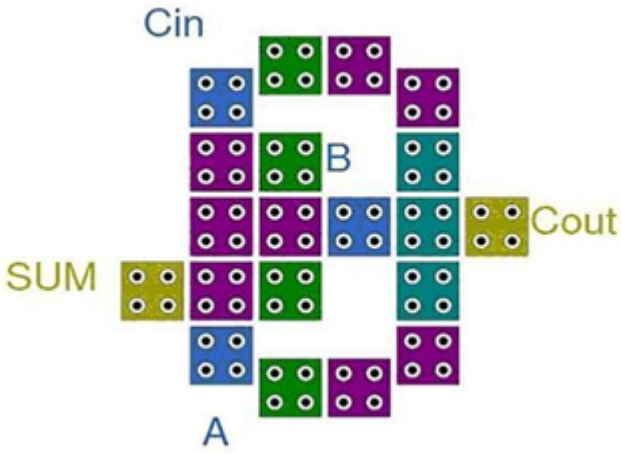

Figure.12 Full adder

Conversely, Table.3 most likely represents the truth table for the whole adder design shown in Figure 12. All potential input combinations and the accompanying outputs are shown in a truth table. An example of how the truth table might be set up for a full adder is given below:

An expansion of the half adder, the full adder may add three input bits to generate sum and carry-out outputs. The full adder circuit consists of multiple QCA-based half

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adders coupled with extra logic gates. To guarantee the complete adder operates efficiently, layout optimisation and carry propagation are carefully taken into account.

Table. 3 Full Adder Truth Table

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4.5. Full Adder Using Two Half Adders

A schematic or layout of a complete adder circuit based on Quantum-Dot Cellular Automata (QCA) and built from two half adders is probably shown in Figure 13, which shows the creation of a full adder utilising two half adders. A complete adder is a digital circuit that generates two outputs, the sum (S) and the carry-out (C_out), by adding three input bits, A, B, and a carry-in (C_in). The complete adder circuit can efficiently compute the sum and the carry-out by employing two half adders.

Two input bits are fed into each half adder, which then outputs a carry-out (C_out) and a sum output (S). The complete adder circuit is built by combining two half adders, one to calculate the sum of A and B and another to calculate the sum of the previous result plus the carry-in (C_in).

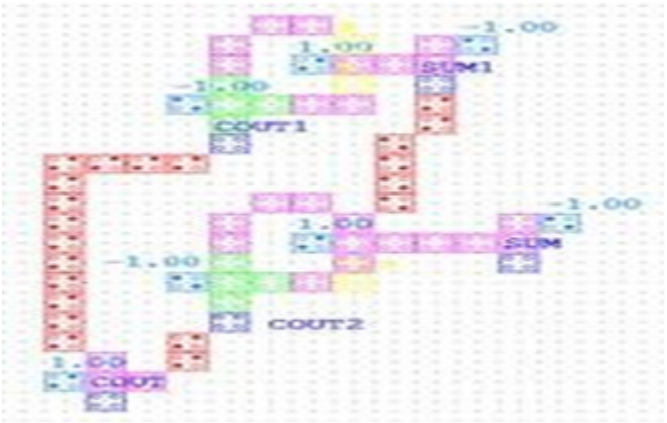

Figure 13 Full adder design using 2 half adders

Using this method, a complete adder is created by joining two QCA-based half adders. Compared to creating a whole adder from scratch, this method can achieve higher performance and density by pooling resources and optimising the layout. Integrating more logic into the design can be necessary to effectively handle carry propagation. This is a theoretical justification of the truth table's possible configuration for a 4-bit binary full adder.

Table IV most likely corresponds to the truth table for the whole adder design shown in Figure 13. All potential input combinations and the accompanying outputs are shown in a truth table. An example of how the truth table might be set up for a full adder using two half adders is shown below.

Table.4 Truth Table for Full Adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4.6. 4-BIT BINARY FULL ADDER

A schematic or layout of a full adder circuit based on Quantum-Dot Cellular Automata (QCA) that can add two 4-bit binary values together is probably shown in Figure 14's design of a 4-bit binary full adder. In order to add each pair of matching bits from the input numbers, take into account any carry-in, and provide the resultant total and carry-out for each bit position, this circuit combines multiple complete adders.

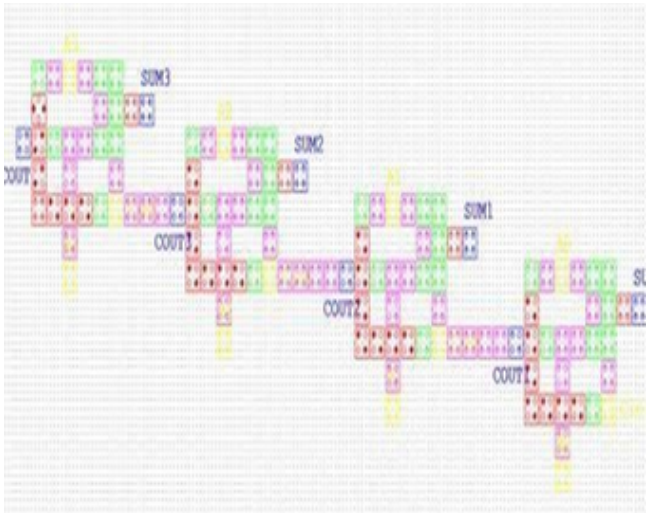

Fig 14: 4 Bit BCD adder

In the 4-bit binary full adder circuit, each full adder calculates the carry-in from the previous bit position as well as the sum and carry-out for one bit position. The 4-bit binary full adder circuit may add four pairs of bits at once by cascading several full adders together.

It is likely that Table V is the truth table for the 4-bit

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binary full adder design shown in Figure 14. All potential pairings of input bits for input numbers and the related outputs are shown in a truth table.

Here's a hypothetical explanation of how the truth table might be structured for a 4-bit binary full adder.

Table. 5 Truth table for 4 bit BCD Adder

	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

A 4-bit binary adder is constructed by cascading circuits together multiple QCA-based complete adders. In order to produce the total and carry-out for that bit location, each full adder stage processes one operand bit in addition to the carry-in from the previous stage.

Optimising layout and carefully routing connections are essential to ensuring the 4-bit adder operates and performs as intended. The project's implementation can be varied overall depending on the components and design techniques selected, but the end result is always the same

: the realisation of a 4-bit binary adder based on QCA that takes advantage of the special qualities of QCA to achieve high-performance and efficient processing.

The schematic or layout of a Quantum-Dot Cellular Automata (QCA) based full adder circuit that can add two 4-bit binary values together is most likely depicted in the design of a 4-bit binary full adder. In order to add each pair of matching bits from the input integers, this circuit combines multiple complete adders. It then takes into account any carry-in and outputs the resultant sum and carry-out for each bit position..

In the 4-bit binary full adder circuit, each full adder calculates the carry-in from the previous bit position as well as the sum and carry-out for one bit position. The 4-bit binary full adder circuit may add four pairs of bits at once by cascading several full adders together.

It is likely that Table V is the truth table for the 4-bit binary full adder design shown in Figure 14. All potential pairings of input bits for input numbers and the related outputs are shown in a truth table.

In the 4-bit binary full adder circuit, each full adder calculates the carry-in from the previous bit position as well as the sum and carry-out for one bit position. The 4-bit binary full adder circuit may add four pairs of bits at once by cascading several full adders together.

5. Experimental Result

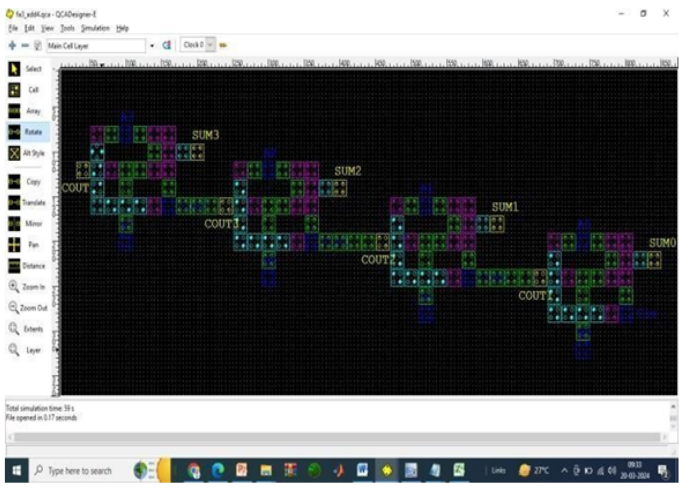

Figure.15 QCA Simulink circuit for 4 Bit BCD Adder

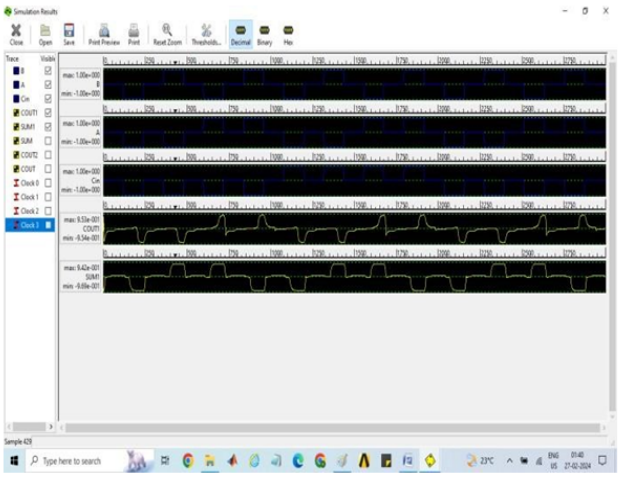

Figure.16 Simulation waveform for 4 Bit BCD Adder

Table.6 Comparison performance for different QCA Designs

S.NO	Design	Total Energy Consumption
1	Inverter using transmission gates	2.86e-003 eV
2	Inverter using gates	1.50e-003 eV
3	Half adder	1.35e-002 eV
4	Full adder	2.19e-001 eV
5	Full Adder using 2 Half Adders	3.96e-002 eV
6	4 Bit Binary Full adder	2.19e-001 eV

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6. Conclusion and Future Scope

Using Quantum-dot Cellular Automata (QCA) technology, a 4-bit binary complete adder was successfully constructed and simulated in this paper. The QCA Designer tool was an invaluable tool for designing and confirming the adder circuit's operation. We created a working 4-bit adder by cascading single-bit full adders in a ripple carry topology.

Examine ways to optimise the design to lower latency and the number of cells. Examine the possibility of designing more intricate arithmetic components, such as multipliers and processors, using QCA.

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