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Design and Implementation of a High-Speed Carry Look-Ahead Adder and Subtractor Using Xilinx ISE

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Abstract: The high-speed carry look ahead adder (CLA), however, has become a very powerful tool for carrying out addition operations quickly in today's computer architecture. Its strong point is its fast processing of binary inputs used to make arithmetic possible .This paper looks at the design principles and benefits that support the high speed CLA in modern computing systems .One of the most impressive attributes of the high-speed CLA is parallelism where carries are generated concurrently with arithmetic operations on binary numbers. Through this feature, computation delays are minimized thereby increasing efficiency especially when dealing with time critical scenarios . Another interesting characteristic of the CLA is its ability to perform consistently even when it comes to inputs having multiple bit widths which makes it suitable for solving more complex computational problems. Additionally, by incorporating XOR gates into the structure, subtraction processes are seamlessly embedded within the CLA, thereby enhancing performance in both addition and subtraction tasks . Although it is mainly used in addition and addition only as a matter of fact, versatility alone makes Carry lookahead Adder an essential building block for many digital circuits.
Keywords: Learning, Chronic Kidney Disease(CKD),Dataset, SVM, Random Forest, ANN.

1. Introduction

The high-speed version of a carry look-ahead adder (CLA) is a crucial component in digital circuit design, allowing for rapid addition and subtraction operations. Unlike a ripple carry adder, which processes each bit sequentially, a CLA can generate carry signals in parallel, significantly reducing the propagation delay and improving overall performance. In this essay, we will delve into the intricacies of the high-speed CLA, exploring why it is preferred over ripple adders, the concept of propagation delay, and a comparison between the two types of adders. History and Key Figures :The concept of carry look ahead adders can be traced back to the pioneering work of mathematicians and engineers in the mid-20th century. In the early days of digital computing, simple adders were constructed using basic logic gates to perform arithmetic operations. However, as the demand for faster and more efficient circuits increased, researchers began to explore new methods to enhance the speed and reliability of addition and subtraction processes . One of the key figures in the development of carry look ahead adders is Hans G. Musmann, who introduced the concept of carry look-ahead techniques in the early 1960s. Musmann's work laid the foundation for the design of high-speed adders that could generate carry signals in advance, eliminating the need for carry propagation through each stage of the adder.

1.1. The High-Speed Carry Look-Ahead Adder

The high-speed version of the Carry Look-Ahead Adder represents an epoch in digital arithmetic circuits characterized by exceptional computational speed and efficiency. Fundamentally, the CLA is based on innovative design principles and parallel processing techniques to reduce the propagation delay and maximize the computational throughput. Unlike the ripple adder, which uses a sequential mode of operation, carries signals are propagated one stage at a time. On the other hand, CLA adders take advantage of the parallelism and precompute carry signals for many stages all at once. This approach not only speeds up arithmetic computations but also increases

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the efficiency of the adder, thus finding applications in high-performance computing.

1.2. Advantages of CLA Over Ripple Adder

The preference for the Carry Look-Ahead Adder over the conventional Ripple Adder is based on its intrinsic advantages of computational speed, efficiency, and flexibility. While ripple adders still rely on sequential processing and carry propagation for executing arithmetic operations, CLA adders use parallelism and proactive carry generation in attaining unprecedented speeds and efficiencies. That is the fundamental difference between CLA and Ripple Adders, setting them apart to prove how CLA is superior to other designs in modern computational applications.

1.3. Propagation Delay

Propagation delay is one of the most essential parameters in any digital arithmetic circuit that affects the speed and efficiency of the arithmetic operation concerned. In the case of a ripple adder, the propagation delay is the time it takes for a carry signal to propagate through each stage of the adder; this forms a cumulatively delayed system that impedes computational throughput. In that way, it imposes major performance limitations on ripple adders, especially in applications where high-speed arithmetic calculations are required .On the other hand, the high speed CLA bypasses propagation delay with the help of innovative design principles and carry generation techniques. Based on the input operands, already computed carry signals make CLA adders free of the carry propagation required during an arithmetic operation, hence reducing propagation delay and enhancing computational efficiency. This inherent advantage of CLA over the Ripple Adder is very important in high-performance computing environments, where speed and efficiency are colossal.

1.4. CLA vs. Ripple Adder

The detailed comparison between the high-speed Carry Look-Ahead Adder and the conventional Ripple Adder reveals the distinctive advantages of CLA in terms of speed, efficiency, and versatility. While Ripple Adders propagate carry signals stage by stage, working in sequence, CLA adders use parallelism and generate carry in advance to achieve extraordinary computational performance. This parallel processing architecture enables CLA adders to outperform Ripple Adders in many computational tasks, especially in time-critical applications that demand rapid arithmetic computations. Moreover, the scalability and flexibility of CLA adders further point out their superiority over Ripple Adders. CLA adders can seamlessly adapt to varying word lengths without compromising speed or efficiency, making them a necessity in a diversity of computing environments. By contrast, Ripple Adders are bound by sequential processing and the delay in propagation that poses constraints on their performance and scalability. The high-speed version of the Carry Look-Ahead Adder is one of the pinnacles of computational efficiency in modern computing systems. Its intrinsic advantages, as contrasted with the conventional Ripple Adder, encompass a minimal propagation delay and parallel processing capability, versatility in performing addition and subtraction tasks, and underscore its significance in advancing digital arithmetic circuits. With the evolution of computational demands, the high-speed CLA remains at the forefront of innovation in advancing computational speed, efficiency, and versatility.

2. Why we Prefer CLA over Ripple ADDER

Arithmetic operations, such as multiplication and division, involve multiple additions or subtractions, and the delay involved in adders due to carry propagation causes a significant problem. This delay contributes to slowness in all arithmetic operations, and it is the emphasis for this delay to be reduced. Among the approaches developed is the carry look-ahead adder. In a carry look-ahead adder, the carry signals are computed in advance according to input signals. The adder then computes the output signals by immediately considering the carry signals, effectively excluding the delay associated with the carry signals. This, in effect, reduces the delay associated with the carry signal and improves the speed of computation. On the other hand, ripple carry adders rely on the carry signals from the previous stages, which results in sequential processing and a significant amount of propagation delay.

Each adder block in the ripple carry adder must wait for the carry signals from the preceding blocks before it can produce its results. Its dependency on previous stages results in cumulative delay which impacts the speed of arithmetic operation. The propagation time in a ripple carry adder is the propagation delay of each adder block times the number of blocks in the circuit. For example, if each full adder stage has a delay of 20 nanoseconds, then the final sum value for a 4-bit adder will be settled after 60 nanoseconds (20 nanoseconds times 3 stages).

As the number of stages increases, the propagation delay also increases, which further causes slowness to the arithmetic operation. It is only by reducing carry propagation delay that the speed of arithmetic's can be improved. A carry look-ahead adder computes the carry signals in advance and can efficiently work out addition operations in contrast to the ripple carry adders.

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3. Carry Look Adder

A Carry Look-Ahead Adder (CLA) is a type of digital circuit used to perform fast arithmetic operations, particularly addition, in computer processors and other digital systems. Unlike simpler adder designs CLAs use a more complex logic structure to reduce the propagation delay associated with carry signals, enabling faster operation.

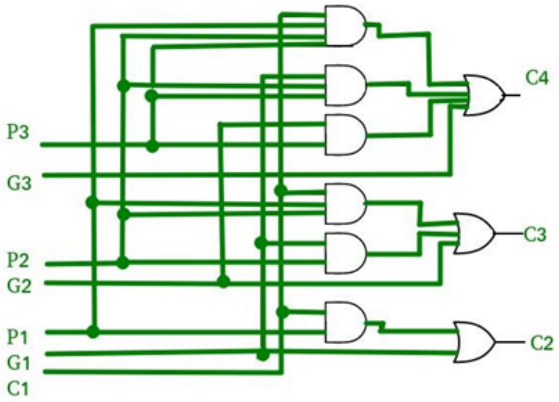

Fig.1 This is the basic block diagram of Carry Look Ahead Adder(source: Geek for geeks)

If we look into the block diagram of the Carry Look Ahead Adder, we have a combinational circuit block where it generates the carries for all the addition blocks.

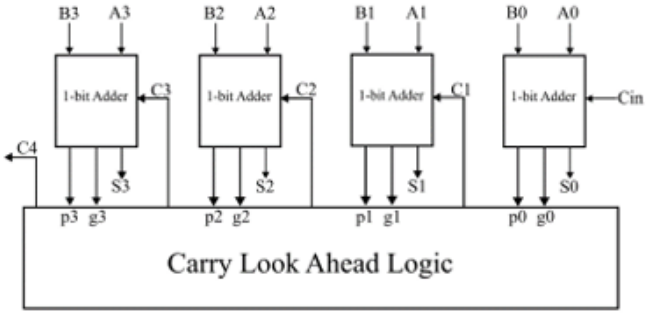

Fig.2 Block Diagram of Carry Look Ahead Adder

In a CLA, the carry-in and carry-out signals for each bit position are computed in parallel rather than sequentially. This parallel computation is achieved by generating "look-ahead" carry signals based on the input operands, allowing for faster determination of the carry status for each bit position. In this CLA we have G=carry generate and P=carry propogate

$$P_i = A_i \oplus B_i$$
$$G_i = A_i B_i$$

The output variable(Sum, Carry) expressions of CLA are (source: Geek for Geeks)

$$S_i = P_i \oplus C_i$$
$$C_{i+1} = G_i + P_i C_i$$

A	B	Ci	Ci+1	Condition
0	0	0	0	No carry generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No carry propogate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry propogate
1	1	1	1	

Truth Table of Carry Look Ahead Adder (source: Geek for Geeks)

The expressions for Boolean functions of carry are (source: Geek for Geeks)

$$C_1 = G_0 + P_0 C_{in}$$
$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_{in}$$
$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}$$
$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{in}$$

The key advantage of a CLA is its ability to reduce the critical path delay, which is the maximum time required for a signal to propagate from the inputs to the outputs. This reduction in delay enables faster addition of multi bit numbers, crucial for high-performance computing applications. The logic equations used in a CLA involve both "generate" and "propagate" signals, which determine whether a carry must be generated locally at each bit position or propagated from lower-order bits. By efficiently combining these signals, a CLA can determine the carry status for each bit position in constant time, regardless of the number of bits being added.

4. How to Implement Subtraction Operation Using Carry Look Ahead Adder

Carry Lookahead Adders (CLA) are known for their efficiency in performing fast addition operations within digital circuits. However, their potential doesn't stop at addition alone. With modifications, CLAs can also serve as subtractors, offering a versatile solution for high-speed arithmetic operations. The fundamental operation of a Carry Lookahead Adder as an adder is paramount to understanding its application as a subtractor. CLAs excel in parallel addition by pre computing carry signals, significantly reducing the propagation delay which became a problem in traditional ripple carry adders.

This carry generation enables CLAs to offer high performance in terms of speed and efficiency. To extend the functionality of CLAs to subtraction, certain modifications are required. First, one of the operands needs to be complemented to transform the subtraction operation into an addition operation

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with a two's complement. This can be achieved through XOR operations or dedicated complementor circuits. Second, the initial carry must be modified to be set to 1 instead of 0, ensuring that the subtraction operation begins with a borrow, mimicking the two's complement subtraction.

Finally, additional control logic is necessary to indicate the operation mode and handle operand complementation and initial carry modification. Each bit of B is XORed with the mode control signal Sub (0 for addition, 1 for subtraction). Here the B input data is 2's complemented using XOR gate.

$$B_i' = B_i \oplus 1$$

$$G_i = A_i \cdot B_i'$$

$$P_i = A_i \oplus B_i'$$

The total output variable expression of the CLA adder and subtractor are

$$S_i = A_i \oplus B_i' \oplus C_i$$

$$C_{i+1} = G_i + (P_i \cdot C_i)$$

The total Sum and Carry individual expressions are

$$S_0 = A_0 \oplus B_0' \oplus \text{Sub}$$
$$S_1 = A_1 \oplus B_1' \oplus C_1$$
$$S_2 = A_2 \oplus B_2' \oplus C_2$$
$$S_3 = A_3 \oplus B_3' \oplus C_3$$

$$C_1 = G_0 + (P_0 \cdot \text{Sub})$$
$$C_2 = G_1 + (P_1 \cdot C_1)$$
$$C_3 = G_2 + (P_2 \cdot C_2)$$
$$C_4 = G_3 + (P_3 \cdot C_3)$$

Now, let's take a look at the truth tables For SUB = 0 (Addition Operation)

A	B	SUB	Sum	C4
0000	0000	0	0000	0
0001	0001	0	0010	0
0010	0010	0	0100	0
0011	0011	0	0110	0
0100	0100	0	1000	0
0101	0101	0	1010	0
0110	0110	0	1100	0
0111	0111	0	1110	0
1000	1000	0	0000	1
1001	1001	0	0010	1
1010	1010	0	0100	1
1011	1011	0	0110	1
1100	1100	0	1000	1
1101	1101	0	1010	1
1110	1110	0	1100	1
1111	1111	0	1110	1

For SUB = 1 (Subtraction Operation)

A	B	SUB	Sum	C4
0000	0000	1	0000	1
0001	0001	1	0000	1
0010	0010	1	0000	1
0011	0011	1	0000	1
0100	0100	1	0000	1
0101	0101	1	0000	1
0110	0110	1	0000	1
0111	0111	1	0000	1
1000	1000	1	0000	1
1001	1001	1	0000	1
1010	1010	1	0000	1
1011	1011	1	0000	1
1100	1100	1	0000	1
1101	1101	1	0000	1
1110	1110	1	0000	1
1111	1111	1	0000	1

Then, CLAs can perform subtraction operations at high speed. The carry lookahead mechanism allows for the simultaneous computation of carry signals across multiple stages, eliminating the need for carry ripple propagation and further enhancing speed.

The application of CLAs as high-speed subtractors finds utility in various domains. In digital signal processing (DSP), for example, algorithms often involve complex arithmetic operations, including both addition and subtraction. CLAs with subtraction capability facilitate rapid computation of DSP algorithms, enabling real-time processing of signals in applications such as audio and image processing.

Similarly, in cryptography, where arithmetic operations are fundamental to encryption and decryption, CLAs as subtractors play a crucial role in executing cryptographic algorithms efficiently, ensuring secure communication and data protection. Carry Lookahead Adders, known for their high-speed addition capabilities, can be effectively utilized as subtractors with appropriate modifications.

By incorporating operand complementation, initial carry modification, and additional control logic, CLAs can perform subtraction operations safely and efficiently. This versatility makes CLAs indispensable in high-speed computing applications across diverse domains, ranging from digital signal processing to cryptography and scientific computing.

5. How can we create a High-Speed Version of Carry Look Ahead Adder and Subtraction

High-speed Carry Look-Ahead Adders are capable of adding and subtracting. A number of strategies would have to be employed to make it very fast. The advanced synthesis of logic minimizes gate delay and optimizes the critical path.

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The designing the logic equations for the generation of carry and sum computation is done to minimize the logic levels and propagate delay time. This decreases the latency of the adder. The high-speed transistor-level design methodology can be employed to increase its speed. Advanced techniques of dynamic logic and domino logic offer faster signal propagation than static CMOS logic.

Results of CLA Adder and Subtractor in Xilinx ISE

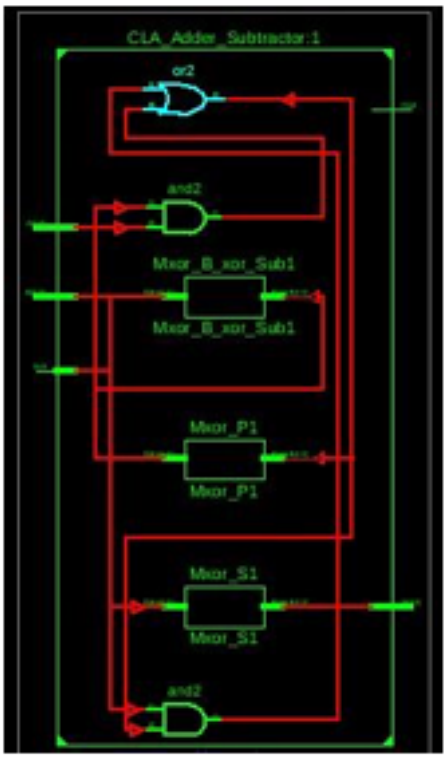

Fig.3 The internal structure of the RTL view Block diagram

Dynamic transistor behaviour results in higher clock frequencies and lower gate delay, thereby increasing the overall adder speed. By computing the carry bits in parallel, rather than in a sequential manner, the overall carry propagation time can be reduced, hence speeding up addition and subtraction operations. This can be realized by the partitioning of the adder into smaller blocks and performing carry computation simultaneously across all blocks.

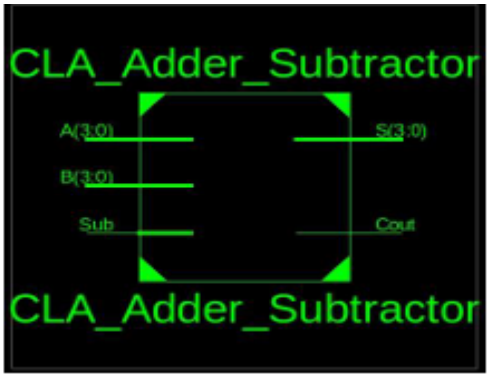

Fig. 4 The block diagram of the CLA Adder and Subtractor

High-speed arithmetic components, such as high speed full adder cells, can be exploited to improve the overall adder speed.

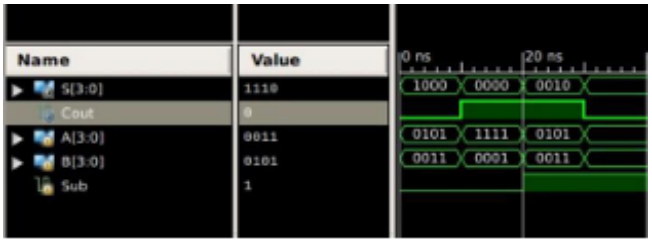

Fig.5 The result waveform of the CLA adder and subtractor in Binary format

These cells are optimized to have the least switching time of transistors and minimize the propagation delay, thereby making the arithmetic operations fast. Besides, the possibility to utilize advanced technologies of semiconductor fabrication will allow adder construction with higher speeds of transistor switching and lower power consumption

Fig.6 The result waveform of the CLA adder and subtractor in Decimal format.

Table.1 Comparison of CLA's[1]

Adder Name	Critical Path Delay (n sec)
RCA	3.40
Conventional CLA	2.53
Ling Adder	2.39
Proposed CLA	1.566
Conditional Sum Adder	1.71

If we Observe the above table we can conclude that proposed High Speed Carry Look Ahead Adder and Subtractor is very fast .In the proposed CLA the critical path delay is very less as compared to remaining traditional CLA's. This Carry look ahead adder and subtractor is designed in such a way that it can generate the output very fast comparing to traditional CLA's.

6. Conclusion and Future Scope

The future scope for high-speed carry look-ahead adders and subtractors includes improvements in CPU performance, better handling of digital signals, and faster cryptographic algorithms. They will also contribute essentially to artificial intelligence in

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supporting high performance computing in scientific research. Moreover, future optimization techniques of emerging technologies will further increase the efficiency and scalability of high speed carry look-ahead adders and subtractors.

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