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DESIGN AND SIMULATION OF FREQUENCY BOOST JITTER REDUCTION FOR VCRO

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Abstract- *Ring oscillators (ROs) are popular due to their small area, modest power, wide tuning range, and ease of scaling with process technology. Due to their poor phase noise and jitter performance, its applications are limited. Both thermal noise and flicker noise contribute jitter that inversely decreases the oscillation frequency. This describes a frequency boost technique to reduce jitter in ROs to boost the internal oscillation frequency and to introduce a frequency divider that follows the oscillator to maintain the desired output frequency. This approach offers reduced jitter as well as the opportunity to trade off output jitter with power for dynamic performance management. The highest oscillation frequency achieved is 45.361Ghz with a root-mean-square period jitter of 4.9725ns and a power consumption of 5.3441mW at 3.3V supply. A jitter model for current-starved oscillators was derived and verified and direct relationship between oscillation frequency and jitter was derived and measured. Compared with other oscillators, this design achieves performance in terms of jitter and figure-of-merit.*

Keywords- *VCRO, Frequency, Simulation*

1 INTRODUCTION

Voltage-Controlled oscillators (VCOs) are fundamental building blocks for many VLSI systems and are widely used in many timing applications. Current-starved ring oscillators (ROs) are popular as they offer a reasonable balance between area, power, and phase noise, in addition to having the widest tuning range. In comparison with other popular VCO architectures, such as the LC-tank oscillator, the compact design and easy integration of ROs make them attractive, especially in monolithic VLSI systems. Furthermore, these benefits of ROs scale with technology, making them even more attractive in advanced technologies. However, ROs are generally considered to have poor phase noise and jitter performance that adversely affects the system performance. This paper presents a jitter reduction technique to allow more VLSI systems to utilize ROs, which in turn should provide better performance for monolithic systems.

Most of the existing techniques to reduce jitter and phase noise in ROs involve putting an RO in a phase-locked loop (PLL) and relying on the PLL to correct and confine timing and phase error. These techniques focus on minimizing the RO-induced noise in the loop but not on reducing the intrinsic noise. A slew rate balancing circuit equalizes the rising and falling slew rate of the oscillator and, thus, improves the symmetry of the output waveform, so that the up-converted flicker (1/f) noise is minimized. A dual control VCO and a fourth-order PLL were used to stabilize VCO gain over process variations and frequency shifts, which in turn maintained the PLL bandwidth to improve jitter performance. Similarly, the dual control technique was used to minimize VCO gain and maximize loop bandwidth to reduce jitter while maintaining a wide frequency range. However, use of a PLL requires a reference signal, which may not be available in all systems. There are other techniques that do not require a PLL, but can potentially be incorporated into a PLL to further improve jitter performance. One such method is a phase-aligning technique that periodically realigns the output to a clean reference so that the jitter does not accumulate over a long period. Another approach maximizing the output amplitude of the oscillator was found useful to improve phase noise and suppress noise current.

A similar study showed that fast rail-to-rail switching reduces phase noise. Jitter can also be reduced by minimizing the number of active devices so as to minimize noise sources [1]. Supply regulation is also important for ROs, because supply noise modulates directly into ROs and induces timing error. Design parameters can be optimized to reduce the intrinsic noise-induced jitter by understanding their governing relationships.

This project describes a novel frequency-boost technique to reduce jitter in ROs. Following the last set of techniques above, we have observed that both thermal noise and flicker noise-induced jitters are inversely proportional to oscillation frequency. The fundamental concept of this technique is that boosting the oscillation frequency achieves low jitter in conjunction with a frequency divider (FD) that adjusts the RO output to the desired output frequency. An oscillator followed by an FD is widely used but rarely are they designed as one unit and their overall performance reported. The FD has to be carefully designed to add minimal jitter to ensure that the overall jitter performance is better than that of a comparable non-frequency-boosted design. Expected performance has been confirmed using theoretical analysis and verified with measurement results.

This project is organized as follows. Section II explains the theoretical basis of the frequency-boost technique and its mechanism of jitter reduction as well as the effect of frequency division on jitter. The prototype circuit and discusses frequency

sensitivity in its bias generation, the measurement results of frequency sensitivity, jitter, power, and power- and frequency normalized jitter figure-of-merit (FOM) are described below [2]. The derivations of jitter and FOM for the current-starved RO are given in the Appendix. The main contributions of this project are the novel frequency-boost jitter reduction technique, its theoretical and experimental verification, an improved jitter model for the current-starved RO, and the presentation of the direct relationship between oscillation frequency and jitter for ROs. For the purposes of lowering jitter (or increasing FOM), this technique can be applied to any oscillator whose dominant jitter variance is inversely proportional to oscillation frequency (oscillation frequency squared).

2 LITERATURE REVIEW

Frequency-boost technique

A continuous-time filter is operable to boost of an input signal including a first integrator to input the input signal and to integrate the input signal and to output a first integrated signal, a second integrator coupled to the first integrator to input the first integrated signal and to integrate the first integrated signal and to output a second integrated signal, and a third integrator coupled to the second integrator to input the second integrated signal and to integrate the second integrated signal and to output a third integrated signal.

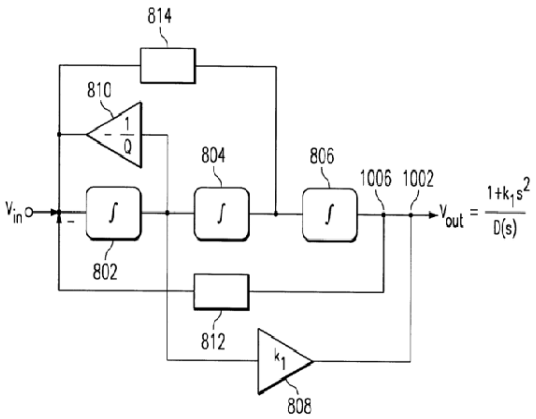

Fig 1: illustrates the effects of the programming of bandwidth without boost

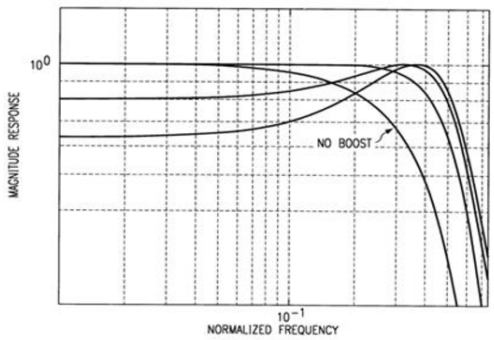

Fig 2 : illustrates the effect of boost programming with one bandwidth setting

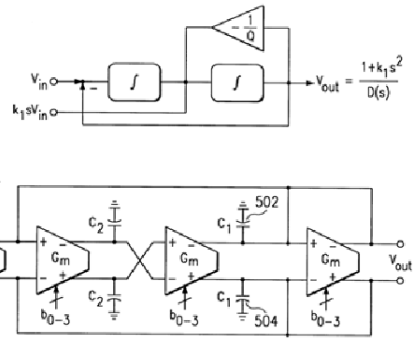

Fig 3: DC gain of the filter

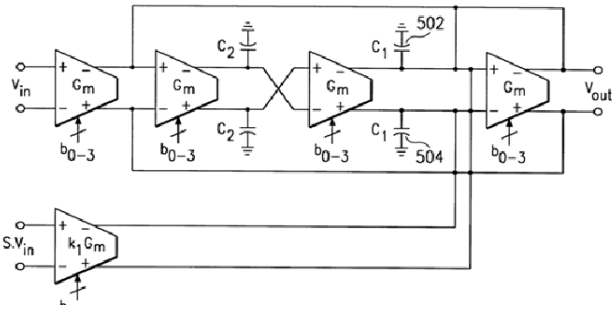

Fig 4:Schematic of conventional boost circuit

Types of oscillators:

Background: Electronic oscillators and the criteria for sustainable oscillations. An electronic oscillator has a gain element and a feedback element.

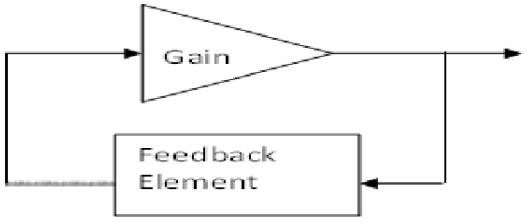

Fig 5: Electronic oscillator

Modified jitter model

Improvement of the New Jitter Model

The new jitter model improves upon the prior model (A1) and (A2). In the old model, the design parameters cannot be varied arbitrarily; parameters IINV, LN, VDD, and fosc have a relationship similar to the current starved RO as in (A10), which introduces constraints among these parameters. The new model introduces an approximation of effective loading capacitance for the inverters in the RO and imposes this as a constraint to determine the relationship among these parameters [3]. Parameter ICSI is then replaced with the other three parameters. Thus, the design parameters in the new model can be varied arbitrarily unless the corresponding ICSI is physically impossible to achieve. This yields a more intuitive and straightforward model. As a result, the model is a function of fosc, VDD, noise coefficients, design geometry (N, WN, and LN), and constants. The model predicts jitter accurately over the entire operating range of the circuit.

Design Guidance for Current-Starved RO Design

The exploration of design space allows us to draw some conclusions and offer design guidance for current-starved ROs. Suggest that, to minimize jitter without power constraints, higher values of N and M

corresponding to more inverter stages and DB2 stages higherfosc) are generally better at a fixed output frequency. However, in that case, the maximum output frequency is strictly limited. This is consistent with the jitter model. The model suggests that in order to minimize jitter at a fixed output frequency, we need to have higher N, M, VDD, WN /LN , and L, but lower WN,CS/LN,CS. Equation (A18) suggests that, as long as the desired output frequency can be achieved, the circuit should be configured to the highest N and M with a priority for M, given the stronger dependence on M than N.

Summarizes the N and M values that minimize jitter from measurements at different output frequencies. We also use (A18) to predict which (N, M) combinations minimize jitter as a function of frequency. The measured optimal values were determined using linear regression in the log domain to approximate the data for each mode (average slope was used for modes with only one data point) at specific frequencies. The order matches the theoretical model.

Technology Dependence

Detailed derivation for the FOM of an RO may be found in the Appendix. The power of auxiliary circuits, such as the PLL or FD, was not considered. The process parameters used here were from SPICE models released by the foundry. In the calculation, we assume that both thermal and flicker noise coefficients are constant across technologies[4].

To understand more precisely the effects of technology scaling, variations in noise coefficients need to be considered. Studies have demonstrated that thermal noise coefficients, γN and γP, are relatively insensitive to technology but increase for short channel devices. However, the coefficients increase by less than 2× from channel lengths of 500 to 40 nm, by less than 1.5× from 240 to 100 nm, and less than 20% from 2 μm to 200 nm. On the other hand, flicker noise coefficients, K f N and K f P, are insensitive to channel length but depend on technology. However, they vary less than 50% across 0.35-, 0.25-, and 0.18-μm technologies.

Applications of Frequency-Boost Technique

The frequency-boost technique generally applies to standalone ROs or ROs incorporated into PLLs. However, when incorporated into a PLL, special attention should be paid to the overall PLL stability performance, because frequency division is equivalent to scaling the VCO gain; loop characteristics should be adjusted accordingly to optimize stability.

For the purposes of lowering thermal and flicker noise-induced jitter in standalone ROs, this technique is valid for ROs meeting these two conditions: maximum oscillation frequency is higher than the targeted output frequency, so there is room to allow frequency division and the dominant jitter variance is inversely proportional to the oscillation frequency raised to a power greater than one.

The benefit of this technique is greater if the frequency dependence is stronger. For the purpose of achieving better FOM, the first condition still holds while the second condition becomes stricter. The dominant jitter variance should be inversely proportional to the oscillation frequency raised to a power greater than two under the assumption that power scales linearly with oscillation frequency.

A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits [1]-[6]. There are many different implementations of VCOs. One of them is a ring oscillator based VCO, which is commonly used in the clock generation subsystem. The main reason of ring oscillator popularity is a direct consequence of its easy integration. Due to their integrated nature, ring oscillators have become an essential building block in many digital and communication systems [5]. They are used as voltage controlled oscillators (VCO's) in applications such as clock recovery circuits for serial data communications, disk-drive read channels, on-chip clock distribution, and integrated frequency synthesizers.

The design of a ring oscillator involves many tradeoffs in terms of speed, power, area, and application domain. The problem of designing a ring oscillator is in focus of our interest in this paper. This paper proposes a suitable method for increasing frequency stability of a CMOS ring VCO. The rest of the text is organized as follows. In chapter 2, we given a brief review of voltage controlled ring oscillators, and define some crucial operating parameters. Hardware description of the proposed ring oscillator is presented in following. In addition we present the simulation results which relate to frequency stability in terms of temperature and supply voltage variation.

Ring oscillator inverting stage

As we have already mentioned, the ring oscillators is realized with N inverter stages. There are numerous types of inverter stages by which a ring oscillator can be realized [8], [9]. Some of the standard solutions are pictured in Fig. 3. Designs given in Fig. 3 b), c), d) are of current starved type, for which the charging and discharging output capacitor current is limited by a bias circuit. More details related to realization of this type of inverter stage can be found in References [8], [9].

Relative frequency deviations in term of temperature variations for 3-stages ring oscillators based on type of inverters stages presented in Fig. 3 are given in Fig. 4. In general all frequency deviations have similar behavior, but the basic type (Fig. 3 a)) and current starved with symmetrical load (Fig. 3 d)) inverters have the highest, while current starved with output-switching (Fig. 3 b)) inverter has the lowest sensitivity. The ratio ofrelative frequency deviations between basic type (Fig.3.3 a)) and current starved with output-switching (Fig.3. 3 b)) inverters is 5:1.

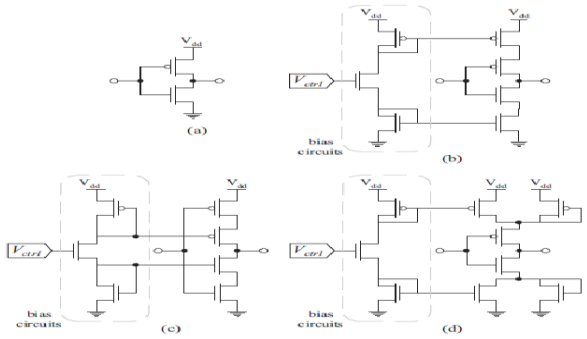

Fig 6:Inverter: (a) basic type (b) current starved with output-switching (c) current starved with power switching; (d) current starved with symmetrical load.

Relative frequency deviations in term of power voltage supply variations for 3-stages ring oscillators based on type of inverters stages presented in Fig. 3 are given in Fig. 5. As can be seen from Fig 5, the basic type (Fig.

3(a)) and current starved with symmetrical load (Fig. 3(d)) inverters have characteristics with negative slope, while current starved with output-switching (Fig. 3 (b)) and current starved with power-switching (Fig. 3 (c)) inverters have characteristics with positive slope. Absolute value of inverters sensitivity in function to power supply voltage variation is within a range of 10% excluding current starved inverter with power-switching (Fig. 3 c) inverters which has sensitivity of 5%.

Taking into consideration the opposite slope characteristics of the relative frequency deviations in terms of power voltage supply variations of the mentioned inverters (Fig. 5), we can conclude that is reasonable to design a ring oscillator composed of cascade chain of inverters.

For example, odd numbered inverters can have positive, while even numbered negative slope. In this way, the relative frequency deviation in term of power voltage supply can be drastically reduced (more than 100%). Several typical design solutions of 3-, 5- and 7- stages ring oscillators with reduced sensitivity are given in Fig. 6 a), b) and c), respectively. We call them as combined ring oscillators.

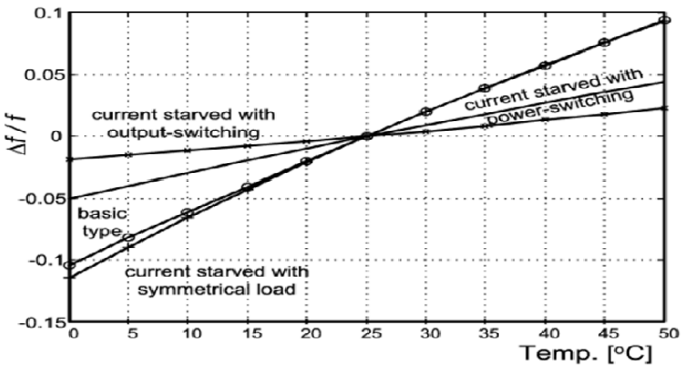

Fig 7:Relative frequency deviation in term of temperature variation

Let note that in combined ring oscillators the odd numbered inverter stages are implemented with basic type, while even numbered as current starved with output-switching inverters.

The relative frequency deviations in term of power supply voltage for all three type of ring oscillators pictured in Fig. 6 are given in Fig. 7. By analyzing the results presented in

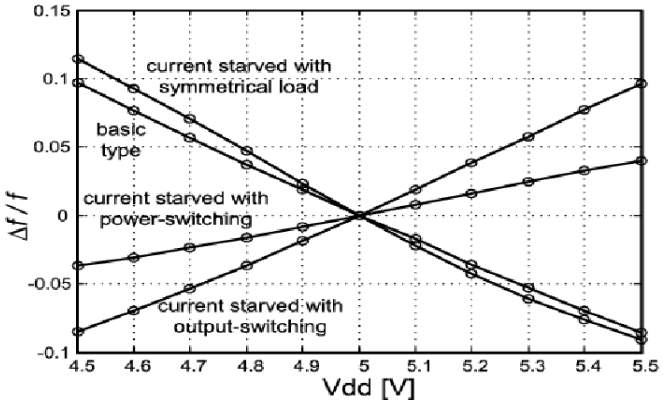

Fig. 8 we can conclude the following: The relative sensitivity of the ring oscillator from Fig. 6 a) is less than 2%, while for Figure-Relative frequency deviation in term of power supply voltage variation those given in Fig. 6(b) and (c) is less than 1%.

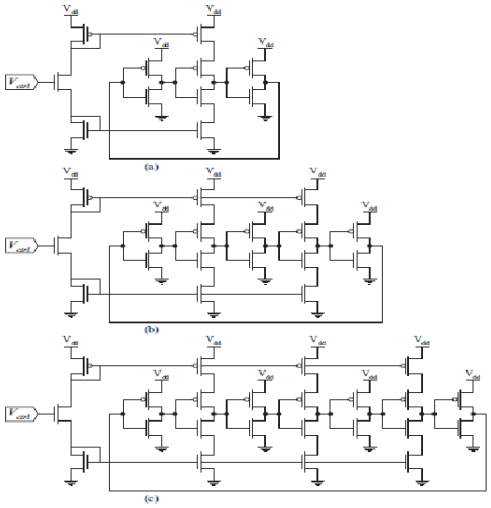

Fig.9: Combined ring VCOs Figure- Relative frequency deviation in term of power supply voltage variation for proposed ring VCOs

Jitter and phase noise in ring oscillators

In general, CMOS circuits are sensitive both to power supply and temperature variations, as well as to noise generated in IC's building blocks (noise is inserted through power supply and the substrate). Due to these effects, the propagation delay, td, is variable [10], [11], [12]. As a consequence there are variations in td, in respect to its nominal value. This deviation is manifested as variation of the rising and falling pulse edges, and is referred as jitter (see Fig. 8).

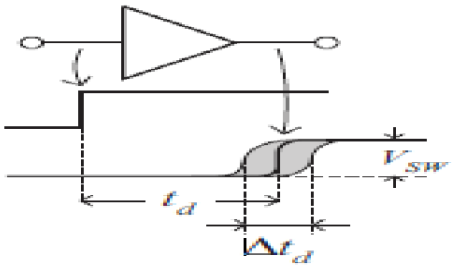

Fig 10: Jitter effect

As can be seen from Fig. 8 the jitter for the rising edge is defined as a rms time error value, $\overline{\Delta td^2}$. The normalized jitter value is defined as a ratio between the effective time error and its nominal delay value, i.e.$\frac{\Delta t_{drms}}{t_d}$. Consider now a VCO with nominal period T0, and with a timing error accompanying each period that is Gaussian, with zero mean and variance $\overline{\Delta t_{VCO}}^2$. If this timing error is expressed in terms of phase, $\Delta\Phi = 2\pi\Delta t/T0$, then the variance of the phase error per cycle of oscillation is given by [10]

$$\sigma_\Phi^2 = (2\pi)^2 \left(\frac{\Delta T_{VCOrms}}{T_0}\right)^2 \qquad (7)$$

The amount of phase noise for all types of ring oscillators discussed in this paper is sketched in Fig. 9. By analyzing Fig. 9 we can conclude that the best performance (phase noise approx. 0.06 rad) have ring oscillators based on current starved inverters with output switching, while the worst (phase noise approx. 0.3 rad) correspond to ring oscillators realized with basic type or current starved with power-switching inverters. Combined

ring oscillators, composed of basic and current starved with output-switching inverters, have approximately phase noise within the range 0.16-0.2 rad.

Current-Starved Ring Oscillator

A). Gated Current-Starved Inverters: The RO consists of nine stages of current-starved inverters. Each inverter has an nMOS switch to ground at the bottom to turn it ON or OFF, as shown in Fig. 2(a). Unused components are disabled to ensure they do not consume power and contribute additional noise to the rest of the circuit.

B). Bias Generation: In this design, we use a pMOS input transistor for converting control input voltage to current [see Fig. 2(b)]. A source-degeneration resistor is used to increase the linearity of the input voltage to control current. pMOS has the potential to achieve lower frequency sensitivity to power supply voltage compared with nMOS.

The converted current is

$$I_{CSI} = \left[V_x + \frac{1}{\beta_p R} + \sqrt{\frac{2V_x}{\beta_p R} + \frac{1}{(\beta_p R)^2}} \right] \Big/ R \qquad (9)$$

Where Vxis defined as VDD − Vin − Vtp, Vtp is the threshold voltage of the input pMOS, and βP is the transconductance parameter of the input pMOS. Inserting (9) into (1), we obtain the oscillation frequency. The frequency sensitivity to supply voltage is defined as Sp= (∂ fosc/∂VDD)/ fosc and can be expressed as

$$S_P = \frac{V_{SW}\left(\frac{2}{\beta_p R\sqrt{\varepsilon}} + 1\right) - \delta\left(V_X + \frac{1}{\beta_p R} + \sqrt{\varepsilon}\right)}{V_{SW}\left(V_X + \frac{1}{\beta_p R} + \sqrt{\varepsilon}\right)} \qquad (10)$$

Where ε is defined as 2Vx /βp R + 1/(βpR)2 and δ is defined as dVSW/dVDD. In (9), we have neglected the dependence of Vtp on VDD due to body effect for simplicity. For most cases, the oscillator switches rail to rail and thus, VSW equals VDD. Following the method above, the frequency sensitivity to supply voltage using an nMOS input transistor SN is −1/VDD. Comparing the absolute values of these two sensitivities, SP is lower than SN when Vin is less than VDD/2−Vtp and absolute Spis the lowest when Vin is 0 V.

Thus, the frequency sensitivity can be reduced using a pMOS as an input transistor. The frequency-boost technique benefits from this reduced frequency sensitivity, because it tends to make the oscillation frequency higher, which is equivalent to a higher current and a lower Vin using a pMOS input. Therefore, the oscillators will mostly operate in a low sensitivity region using the frequency-boost technique. If jitter is found from frequency sensitivity using the jitter derivation for flicker noise, this lower frequency sensitivity to supply translates to lower jitter due to supply noise[6].

All the derivations above assumed that Vin is a ground-referenced control. If a supply referenced control (Vin shifts with VDD) is used, the frequency sensitivities found for the two different input transistors are opposite of that derived above.

Frequency Dividers

The DB2 circuit is a transmission gate-based D-flip-flops (DFF) with its inverted output connected to its D input and using CLK and Q as input and output, respectively. The DFF has an nMOS switch to ground to enable it. The FD yields the output frequency Fout = 2−M· fosc, where M is the number of DB2 stages. At the end of the FD is a desynchronizing DFF. It resample's R the divided signal based on the oscillator signal to minimize the jitter contribution of the divider.

Control Generator and Switching Circuit

The control generation circuit uses digital logic gates. Control signals are generated based on two controls, N and M. N has two bits and controls the number of stages used in the RO; M has three bits and controls [7] the number of DB2 stages used in the FD. As a result, the circuit has a total of 32 modes with the number of inverter stages and the number of DB2 stages varying. The mapping between N, M, and internal signals is listed in Tables I and II, respectively. Switches are used to reconfigure the circuit based on the control signal. The 7-1 switch has seven 1-1 switches, each controlled by one bit of Sm. In combination with the power gating technique, this approach ensures that unnecessary switching does not occur, and unused components do not consume.

N	S_{n1-4}	EN_{n2-4}
3	1000	000
5	0100	100
7	0010	110
9	0001	111

Table1: control generation for voltage-controlled ro

M	S_{m0}	S_m	EN_{m1-7}
0	1	0000000	0000000
1	0	1000000	1000000
2	0	0100000	1100000
3	0	0010000	1110000
4	0	0001000	1111000
5	0	0000100	1111100
6	0	0000010	1111110
7	0	0000001	1111111

Table 2: control generation for fd

3 PROPOSED METHOD

Proposed level incremented System diagram of the current-starved Ring Oscillator

The proposed design consists of level incremented current starved R) and FD. By increasing the level of ring oscillator, the frequency increases. This circuit can be applicable for high frequencies.

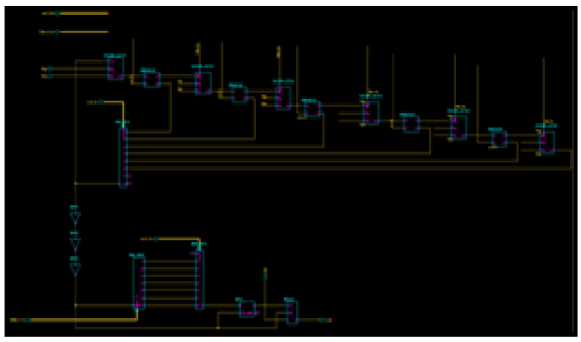

Fig 9:Proposed level incremented System diagram of the current-starved RO (top) and FD (bottom)

Control Generator and Switching Circuit

The control generation circuit uses digital logic gates. Control signals are generated based on two controls, N and M. N has two bits and controls the number of stages used in the RO; M has three bits and controls the number of DB2 stages used in the FD. As a result, the circuit has a total of 36 modes with the number of inverter stages and the number of DB2

stages varying [7]. The mapping between N, M, and internal signals is listed in Tables 3 and 4, respectively. Switches are used to reconfigure the circuit based on the control signal.

The 7-1 switch has seven 1-1 switches, each controlled by one bit of Sm. In combination with the power gating technique, this approach ensures that unnecessary switching does not occur, and unused components do not consume power. The N=11,13 then the selection Sn and En are shown in the table 3. The FD circuit remains unchanged which reduces the jitter.

N	Sn1-4	En2-4
3	100000	00000
5	010000	10000
7	001000	11000
9	000100	11100
11	000010	11110
13	000001	11111

Table 3: Level Incremented Control Generation For Voltage-Controlled R

M	S_{m0}	S_m	$EN_{m1\text{-}7}$
0	1	0000000	0000000
1	0	1000000	1000000
2	0	0100000	1100000
3	0	0010000	1110000
4	0	0001000	1111000
5	0	0000100	1111100
6	0	0000010	1111110
7	0	0000001	1111111

Table 4: Level Incremented Control Generation For FD

Simulation Results

Testbench of jitter

The test bench circuit for proposed design is given in the below figure:

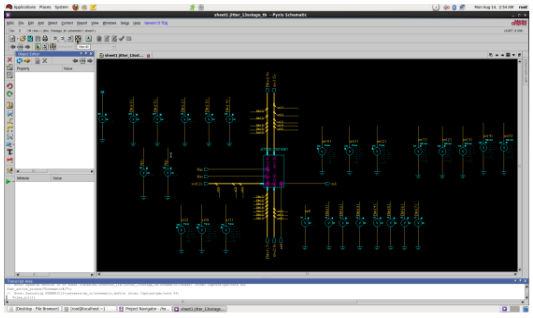

Fig 10:The test bench circuit for the proposed design

Waveform Responses for existing Method

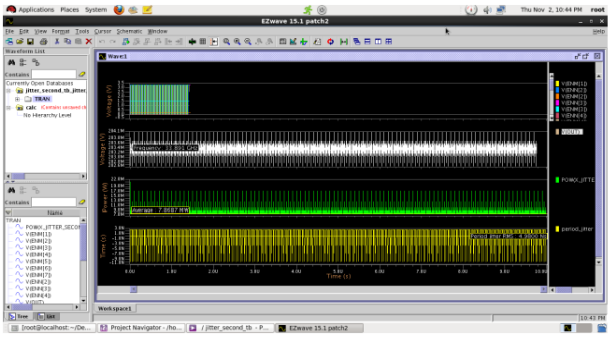

Fig 11: Waveforms for an existing method

The first wave form represents the input signal and the second wave form represents [8] the frequency of the output signal, the third wave represents power consumption and the last wave form is represents the jitter and all the waveforms plotted between voltage and time .

Waveform Responses for Proposed Method

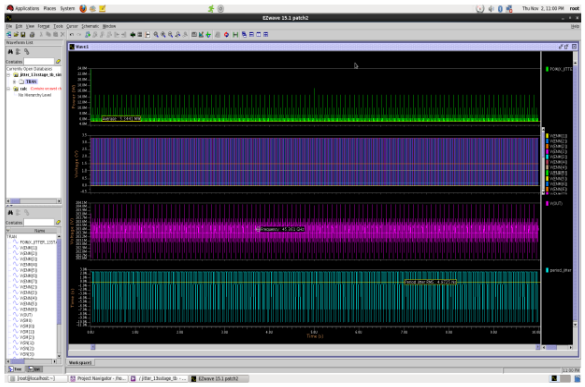

Fig 12: Wave forms for the proposed method

The first wave form represents the power consumption and the second wave form represents input signal and the third wave represents frequency of the output signal, the last wave form is represents the jitter and all the waveforms plotted between voltage and time.

Comparison Table

	Our work	Paper based
Technology	130nm	500nm
Approach	Mixed Signal	Mixed Signal
Design	13 stage RO	9 stage RO
Supply	3.3V	3.3V
Freq	45.361Ghz	33.891Ghz
Power Consumption	5.3441Mw	7.8664mW
RMS jitter	4.9725ns	4.98ns
Power dissipation	5.3417mW	7.8679mW

Table 5:Comparison between existing and Proposed design models

4 CONCLUSION

A frequency-boost technique to reduce jitter is proposed. The frequency and current in the ROs are intrinsically proportional, so we could, alternatively, name it a current boost technique. However, it is more intuitive to understand this technique from a frequency perspective, since the FD was intended for achieving higher internal oscillation frequencies. While this technique has been developed and demonstrated here for an RO, it can apply to any oscillator whose jitter variance is inversely proportional to the oscillation frequency raised to a power greater than one and two for the purposes of decreasing jitter and increasing FOM, respectively.

The reported design consists of a current-starved RO, followed by an FD. A modification to the conventional bias generation was made to improve frequency sensitivity to supply voltage; analysis was also provided. We further derive and verify new models for jitter and FOM. Jitter reduction was verified by measurement results for a chip fabricated in a 0.13-μm CMOS process. Compared with other reported timing signal generators, this design achieved the lowest jitter as quantified by

unit interval and the highest FOM. The performance advantages are expected to readily extend to more advanced technologies.

In Future work, for many high frequency applications the Ring oscillator levels can be further more incremented and the jitter can be reduced by Frequency divider circuit and also be modified depending on the application oriented desire.

References

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